A marked-up version showing amendments to any claims being changed is provided in one or more accompanying pages separate from this amendment in accordance with 37 CFR § 1.121(c)(1)(ii). Any claim not accompanied by a marked-up version has not been changed relative to the immediate prior version, except that marked-up versions are not being supplied for any added claim or canceled claim.

CLAIMS

34. A transistor assembly comprising:

a plurality of active areas having widths defined by shallow trench isolation regions of no greater than about one micron, at least some of the widths being different; and

gate lines disposed over the plurality of active areas to provide individual transistors, those transistors whose widths are different having different threshold voltages from one another.

35. The transistor assembly of claim 34, wherein the threshold voltages of at least some of the individual transistors are less than one volt.

36. The transistor assembly of claim 34, wherein individual transistors having active areas with the smaller widths have threshold voltages which are smaller than other individual transistors having active areas with larger widths.

37. The transistor assembly of claim 34, wherein one of the individual transistors comprises a portion of precharge circuitry for dynamic random access memory circuitry.

38. The transistor assembly of claim 34, wherein one of the individual transistors comprises a pass transistor.

39. The transistor assembly of claim 34, wherein one of the individual transistors comprises a portion of sense amplifier circuitry for dynamic random access memory circuitry and has a lower threshold voltage V_{tl}.

40. The transistor assembly of claim 34, wherein some of the individual transistors are joined together in a parallel configuration.

44. A transistor assembly comprising:

an active area;

a plurality of spaced-apart shallow trench isolation regions received by the active area and defining active sub-areas therebetween, individual active sub-areas having respective widths, at least one of the widths being no greater than about one micron and at least one other sub-area having a width which is different from the one width; and

a gate line extending over the one and the other sub-area and defining, in part, separate transistors, wherein each of the separate transistors has a different threshold voltage.

45. The transistor assembly of claim 44, wherein each active sub-area width of an associated transistor is no greater than about one micron.

46. The transistor assembly of claim 44, wherein each active sub-area width of an associated transistor is no greater than about one micron, wherein more than two separate transistors have different threshold voltages.

47. The transistor assembly of claim 44, wherein said gate line comprises a common gate line which extends over a plurality of the active sub-areas defining a plurality of transistors, each active sub-area width of an associated transistor being no greater than about one micron.

48. The transistor assembly of claim 44, wherein said gate line comprises a common gate line which extends over a plurality of the active sub-areas defining a plurality of transistors, each active sub-area width of an associated transistor being no greater than about one micron and said plurality of transistors being joined in a parallel configuration.

49. A transistor assembly comprising:

an active area;

a plurality of spaced-apart shallow trench isolation regions received by the active area and defining active sub-areas therebetween, individual active sub-areas having respective widths, at least one of the widths being no greater than about one micron and at least one other sub-area having a width which is less than the one width; and

a gate line extending over the one and the other sub-area and defining, in part, separate transistors, wherein the separate transistors have different threshold voltages, wherein said gate line comprises a common gate line which extends over a plurality of the active sub-areas defining a plurality of transistors, each active sub-area width of an associated transistor being no greater than about one micron and said plurality of transistors being joined in a parallel configuration to provide a pull down circuit coupled to a common node.

50. The transistor assembly of claim 49, further comprising a sense amplifier formed from a pair of transistors, each of the pair having a gate that is cross-coupled to a drain of another of the pair, sources of the pair being coupled to the common node.